IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of Priyadarsan PATRA

Group Art Unit: 2825 (Anticipated)

Application No.: TO BE ASSIGNED

Examiner: ANNETTE M. THOMPSON (Anticipated)

Filed: HEREWITH

Docket No.: 2207/1254202

For: NOISE AND POWER OPTIMIZATION IN HIGH PERFORMANCE CIRCUITS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The filing of this Information Disclosure Statement and the enclosed PTO Form No. 1449, shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. § 1.56(b). The paragraphs marked below are applicable. It is believed that no fees other than those indicated below are due, but authorization is hereby given to charge any additional fees due, or to credit any overpayment, to deposit account 11-0600.

■ 1. This Information Disclosure Statement is being filed (a) within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. §1.53(d), (b) within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, (c) before the mailing date of a first Office Action on the merits in the present application, OR (d)

before the mailing of a first office action after filing of a request for continued examination. No certification or fee is required.

❒ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a final action, Notice of Allowance, or any action that otherwise closes prosecution.

❒ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

❒ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

❒ c. Please debit Deposit Account No. 11-0600 in the amount of $180.00 in payment of the fee under 37 CFR §1.17(p) to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached. 37 CFR §1.97(c)(2).

❒ 3. This Information Disclosure Statement is being filed after the mailing date of a final action, Notice of Allowance or an action that otherwise closes prosecution, but before payment of the Issue Fee. Applicant(s) hereby request(s) that the Information Disclosure Statement be considered. Please debit Deposit Account No. 11-0600 in the amount of $180.00 in payment of the petition fee under 37 CFR §1.17(p) to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.

❒ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in any counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

❒ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

■ 4. The reference(s) was/were cited by or submitted to the Office in parent application No.09/964,803, filed September 28, 2001, which is relied upon for an earlier filing date under 35 U.S.C. §120. Thus, copies of these references are not attached. 37 CFR §1.98(d).

Respectfully submitted,

KENYON & KENYON

Date: September 22, 2003

B. Delano Jordan
Registration No. 43,698

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PTO/SB/08A (10-01)
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Sheet 1 of 2

Complete if Known	
Application Number	TO BE ASSIGNED
Filing Date	September 22, 2003
First Named Inventor	Priyadarsan Patra et al.
Group Art Unit	2825 (Anticiaipted)
Examiner Name	Annette M. Thompson (Anticipated)
Attorney Docket Number	2207/1254202

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	TILOS: A Posynomial Programming Approach to Transistor Sizing, FISHBURN, J.P., DUNLOP, A.E. Available from IEEE Service Cent. (Cat. Publ. by IEEE, New York, NY, USA, N 85CH2233-5), Piscataway, NJ, USA p. 326-328.	
	2	Timing driven cell replication during placement for cycle time optimization. NEUMANN, Ingmar and POST, Hans-Ulrich. Integration-The VLSA Journal 27 (1999) pp. 131-141.	
	3	Gate Size Optimization for Row-based Layouts, MAHESHWARI, Naresh and SAPATNEKAR, Sachin S.; Midwest Symposium on Circuits and Systems, Vol. 2 (1995). IEEE, Piscataway, NJ, USA 95CB35853, pp. 777-780.	
	4	Automatic transistor sizing in high performance CMOS logic circuits. HOPPE, B; NEUENDORF, G; and SCHMIDT-Landsiedel D.; VLSI and Computer Peripherals. Available from IEEE Service Cent. (Cat. Publ. by IEEE, IEEE Service Center, Piscataway, NJ, USA., Catalog No. 89CH2704-5), Piscataway, NJ, USA, pp. 5/25-27.	
	5	Timing optimization of mixed static and domino logic. ZHAO, Min, SAPATNEKAR, Sachin S. Proceedings - IEEE International Symposium on Circuits and Systems. v. 6 1998. IEEE, Piscataway, NJ, USA, 98CH36187, pp. 266-269.	
	6	Interleaving Buffer Insertion and Transistor Sizing into a Single Optimization. JIANG, Yanbin; SAPATNEKAR, Sachin S.; BAMJIL, Cyrus; and KIM, Juho; Available from IEEE Service Cent (Cat. Publ by IEEE, New York, NY, USA. 1063-8210/96), Piscataway, NJ, USA, pp. 625-633.	
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